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EXAMINER	
WONG, ALLEN C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,682	KIM ET AL.	
	Examiner	Art Unit	
	Allen Wong	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/28/04 have been fully considered but they are not persuasive.

Regarding lines 11-13 on page 9 of applicant's remarks, applicant argues that Zhang does not disclose a method of adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image as recited in claims 1, 11, 17, 22, 27, 34 and 39. The examiner respectfully disagrees. As stated before in col.9, ln.65 to col.10, ln.25, Zhang discloses calculating the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and the error analyzer calculates a measure of the blocks or the values of variation of the pixel values.

And later on lines 16-20 on page 9 of applicant's arguments, the applicant states that the examiner has provided no basis in Zhang for the examiner's assertion that "the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step". The examiner respectfully disagrees. The examiner's assertion for describing "the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step" is the recursive process of the typical MPEG encoding process for adjusting the quantization

by using data from the buffer 212 after the coder 210 to recursively adjust the quantization so that the image data can be properly encoded at the correct rate so as to accurately, efficiently encode video images in a high quality manner. The recursive quantization control mechanism is not novel and new because it is what typical MPEG encoders do to constantly adjust the quantization parameter, and Zhang teaches this well known concept.

Thus, the rejection of independent claims 1, 11, 17, 22, 27, 34 and 39, and dependent claims 2-10, 18-21, 23-26, 28-33, 35-38 and 40-43 are maintained.

Regarding lines 4-6 on page 10 of applicant's remarks, applicant asserts that Nickerson does not disclose a look up table comprising a relationship between the number of bits and variation in pixel signal values of a plurality of video images for a variety of quantization step sizes as recited in claim 44. The examiner respectfully disagrees. As stated before, Nickerson's col.2, ln.40-52 discloses a storage medium that has one or more quantization lookup tables, in that, for instance, element 508 states quantized coefficient lookup table, and elements 502, 504, 508, 510, 514 of fig.5 are more lookup tables that help the determination of the proper quantization from the quantized coefficient lookup table to correlate the number of bits for encoding a plurality of image data. Further, Nickerson's col.6, ln.49-67, fig.3, element 312 utilizes the data from element 310 where lookup tables are used, as shown in fig.5 which shows the details of element 310, and that element 310 has a table 514 where it takes the number of bits and the variation in pixel signal values into account, and that information is sent to element 312 to generate a set of final Q levels or a set of quantization step sizes to

properly encode the video images by adjusting the quantization step sizes to properly modify the video encoding bit rate. Thus, Nickerson teaches that lookup table 514 takes the number of bits and the variation in pixel signal values of a plurality of video images for a variety of quantization steps into account as disclosed in claim 44.

Regarding lines 16-18 on page 10 of applicant's remarks, applicant mentions that Nickerson does not disclose that lookup table 514 takes the number of bits and the variation in pixel signal values of a plurality of video images for a variety of quantization steps into account as disclosed in claim 44. The examiner respectfully disagrees. The examiner has already replied to this issue in the aforementioned above paragraphs. See the above paragraphs.

Thus, the rejection of claims 44-46 is maintained.

Regarding lines 4-7 on page 11 of applicant's remarks, applicant states that Zhang does not disclose a method of adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image as recited in claim 11. The examiner respectfully disagrees. As stated before in the above paragraphs, in col.9, ln.65 to col.10, ln.25, Zhang discloses calculating the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and the error analyzer calculates a measure of the blocks or the values of variation of the pixel values. Thus, since Zhang discloses a method of adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image as recited in claim 11, it

is reasonable to combine the teachings of Howe into Zhang for suggesting the video encoder is implemented in silicon on at least one integrated circuit (col.6, ln.57-63 and col.17, ln.33-50; video encoding is implemented in silicon on at least one integrated circuit (IC); also, it is well known in the art that integrated circuit chips are implemented in silicon for processing video encoding/decoding tasks), wherein the silicon implementation of the video encoder comprises microcode (col.14, ln.28-43) and firmware (col.17, ln.65-66).

Therefore, it would have been obvious to one of ordinary skill in the art to take Howe's teaching of silicon implementation of a video encoder into Zhang's video compression system for permitting video encoding by use of microcode and firmware via silicon integrated circuits (IC) so as to efficiently encoding video image data in a highly efficient manner. Howe's motivation for combination would be to ensure compatible, cost-effective, efficient, precise, video encoding and decoding of high quality video images for display (col.3, ln.1-13).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Therefore, the rejection of claims 1-46 is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-11 and 17-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang (5,812,195).

Regarding claim 1, Zhang discloses a method of performing video encoding (fig.2) comprising:

adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212).

Regarding claim 2, Zhang discloses the method of claim 1, wherein the selected portion of the video image comprises a macroblock (col.5, ln.33-46; note an image is

subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 3, Zhang discloses the method of claim 2, wherein the video encoding rate is also adjusted based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since they are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since they are obtained by prediction).

Regarding claim 4, Zhang discloses the method of claim 3, where in the type of macroblocks comprise at least one of the following: intra, inter, 4 MV, and B (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type).

Regarding claim 5, Zhang discloses the method of claim 1, wherein the measurement of the variation comprises the sum of absolute differences (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203).

Regarding claim 6, Zhang discloses the method of claim 1, wherein the video encoding rate is adjusted by adjusting the quantization step size employed during

video encoding (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate).

Regarding claim 7, Zhang discloses the method of claim 6, wherein the selected portion of the video image comprises a macroblock (col.5, ln.33-46; note an image is subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 8, Zhang discloses the method of claim 7, wherein the video encoding rate is also further adjusted based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since *intra* frames are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since *inter* frames are obtained by prediction).

Regarding claim 9, Zhang discloses the method of claim 8, wherein the types comprise at least one of the following: intra, inter, 4 MV, and B (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type).

Regarding claim 10, Zhang discloses the method of claim 1, wherein the video encoding performed is substantially MPEG or H.26x compliant (col.3, ln.18-19).

Regarding claim 11, Zhang discloses a device having the capability to perform video encoding (fig.2) comprising:

a mechanism to adjust a video encoding rate employed during the video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212);

wherein said mechanism is implemented within a video encoder (fig.2 is a video encoder that implements the mechanism to adjust the video encoding rate).

Regarding claim 17, Zhang discloses an article (fig.1, element 10 is an article and fig.2 is video encoder) comprising:

a storage medium (fig.1, elements 105 and 106 are storage medium in that the communication and storage system 10 can have access to processor 100, where stored instructions are executed; also, in fig.2, 212 and 214 can store encoded video data), said medium having stored thereon instructions (fig.1, element 106 is a storage unit in that the communication and storage system 10 can have access to processor

100, where stored instructions are executed, and memory 105 can store instructions and other information) that, when executed, result in the performance of video encoding by: adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212).

Regarding claim 18, Zhang discloses the article of claim 17, wherein said medium further has stored thereon instructions that, when executed, result in the selected portion of the video image being encoded comprising a macroblock (col.5, ln.33-46; note an image is subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 19, Zhang discloses the article of claim 18, wherein said medium further has stored thereon instructions, that, when executed, result in the video encoding rate being adjusted also based at least in part on the type of macroblock

(col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since they are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since they are obtained by prediction).

Regarding claim 20, Zhang discloses the article of claim 17, wherein said medium further has stored thereon instructions that, when executed, result in the measurement of the variation comprising the SAD (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203).

Regarding claim 21, Zhang discloses the article of claim 17, wherein said medium further has stored thereon instructions that, when executed, result in the video encoding rate being adjusted by adjusting the quantization step size employed during video encoding (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate).

Regarding claim 22, Zhang discloses a system (fig.1 is a video processing system that includes fig.2 as the video encoder) comprising:

a video encoder (fig.2, element 200 is a video encoder that is part of processor 100 of fig.1);

a video input device coupled to said video encoder (fig.2, note the preprocessing & frame memory 201 receives the video or picture input and also fig.1, element 101); and

memory (fig.1, elements 105 and 106);

wherein said memory is coupled to said video encoder to store video encoded by said video encoder (fig.1, elements 105 and 106 can store video data encoded by the video encoder within processor 100, also, in fig.2, elements 212 and 214 can store the encoded video data); and

wherein said video encoder includes a mechanism to adjust a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212).

Regarding claim 23, Zhang discloses the system of claim 22, wherein the selected portion of the video image comprises a macroblock (col.5, ln.33-46; note an

image is subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 24, Zhang discloses the system of claim 23, wherein the mechanism to adjust the video encoding rate employed during video encoding is also based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since *intra* frames are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since *inter* frames are obtained by prediction).

Regarding claim 25, Zhang discloses the system of claim 22, wherein the measurement of the variation comprises the SAD (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203).

Regarding claim 26, Zhang discloses the system of claim 22, wherein the mechanism to adjust the video encoding rate employed during video encoding is adjusted by adjusting the quantization step size employed during video encoding

(col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate).

Regarding claim 27, Zhang discloses a method of performing video decoding (col.14, ln.60-65; fig.3 is the decoding method for decoding the compressed video data by the encoding method of fig.2) comprising:

decoding video that has been encoded (col.14, ln.60-65; fig.3 is the decoding method for decompressing the compressed video data by the encoding method of fig.2), wherein said encoded video was encoded by adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212).

Regarding claim 28, Zhang discloses the method of claim 27, wherein the selected portion of the video image comprises a macroblock (col.5, ln.33-46; note an image is subdivided into image blocks, where image blocks are macroblocks, since

technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 29, Zhang discloses the method of claim 28, wherein the video encoding rate is also adjusted based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since *intra* frames are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since *inter* frames are obtained by prediction).

Regarding claim 30, Zhang discloses the method of claim 27, wherein the measurement of the variation comprises the SAD (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203).

Regarding claim 31, Zhang discloses the method of claim 27, wherein the video encoding rate is adjusted by adjusting the quantization step size employed during video encoding (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate).

Regarding claim 32, Zhang discloses the method of claim 31, wherein the selected portion of the video image comprises a macroblock (col.5, ln.33-46; note an

image is subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 33, Zhang discloses the method of claim 32, wherein the video encoding rate is also further adjusted based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since *intra* frames are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since *inter* frames are obtained by prediction).

Regarding claim 34, Zhang discloses a system (fig.1 is a video processing system that includes fig.2 as the video encoder and fig.3 as the video decoder) comprising:

a video decoder (col.14, ln.60-65; fig.3 is the video decoder for decoding the compressed video data by the video encoder of fig.2, where the decoder in fig.3 is also encompassed by element 100 of fig.1);

a video output device coupled to said video decoder (col.15, ln.11-13, in fig.3, the output goes to a standard video output such as the display 103 of fig.1, as disclosed in col.7, ln.36-41); and

memory (fig.1, elements 105 and 106);

wherein said memory is coupled to said video decoder to store video previously encoded by a video encoder (fig.1, elements 105 and 106 can store video data encoded by the video encoder within processor 100, also, in fig.3, element 303 can store the video data previously encoded), wherein said video encoder included a mechanism to adjust a video encoding rate employed during the video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212).

Regarding claim 35, Zhang discloses the system of claim 34, wherein the selected portion of the video image comprises a macroblock (col.5, ln.33-46; note an image is subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 36, Zhang discloses the system of claim 34, wherein the mechanism to adjust the video encoding rate employed during video encoding is also

based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since they are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since they are obtained by prediction).

Regarding claim 37, Zhang discloses the system of claim 34, wherein the measurement of the variation comprises the SAD (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203).

Regarding claim 38, Zhang discloses the system of claim 34, wherein the mechanism to adjust the video encoding rate employed during video encoding is adjusted by adjusting the quantization step size employed during video encoding (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate).

Regarding claim 39, Zhang discloses an article (fig.1, element 10 is an article, where fig.2 is the video encoder and fig.3 is the video decoder, and figs. 2-3 are encompassed by fig.1) comprising:

a storage medium (fig.1, elements 105 and 106 are storage medium in that the communication and storage system 10 can have access to processor 100, where stored

instructions are executed; also, in fig.3, element 303 can store the video data previously encoded), said medium having stored thereon instructions that (fig.1, element 106 is a storage unit in that the communication and storage system 10 can have access to processor 100, where stored instructions are executed, and memory 105 can store instructions and other information), when executed, result in the performance of video decoding by: decoding video that has been encoded (col.14, ln.60-65; fig.3 is the video decoder for decoding the compressed video data by the video encoder of fig.2, where the decoder in fig.3 is also encompassed by element 100 of fig.1), wherein said encoded video was encoded by adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203, and later, the results of element 203 is sent to element 204, then to element 205, next to element 210, and then to elements 211 and 212, where element 211 will adjust the video encoding rate by adjusting the quantization step size) and on a bit budget (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 adjusts of the quantization step size for properly adjusting the video encoding rate, wherein the allocation of bits, or bit budget, was taken into account depending on the amount of bits in buffer 212).

Regarding claim 40, Zhang discloses the article of claim 39, wherein said medium further has stored thereon instructions that, when executed, result in the selected portion of the video image being encoded comprising a macroblock (col.5,

ln.33-46; note an image is subdivided into image blocks, where image blocks are macroblocks, since technically, an image is subdivided into 30 slices, and one slice is subdivided into 45 macroblocks, so clearly, the video image comprises a macroblock).

Regarding claim 41, Zhang discloses the article of claim 40, wherein said medium further has stored thereon instructions, that, when executed, result in the video encoding rate being adjusted also based at least in part on the type of macroblock (col.11, ln.62 to col.12, ln.9; an image block or macroblock can be of intra or inter type, and by changing the coding mode depending on the type, this will change the video encoding rate to where if the block is of *intra* type, then *intra*-frame encoding is done and more bits are allocated to encoding intra type blocks because *intra* frames have more detail since they are the original frames, and if the block is *inter* type, then *inter*-frame encoding is done and less bits are required because *inter* frames have less detail since they are obtained by prediction).

Regarding claim 42, Zhang discloses the article of claim 39, wherein said medium further has stored thereon instructions that, when executed, result in the measurement of the variation comprising the SAD (col.9, ln.65 to col.10, ln.25, Zhang discloses the computation of the measurement of the sum of absolute values of the error signal (differences), variation of pixel values, or the SAD is done by error analyzer 203).

Regarding claim 43, Zhang discloses the article of claim 39, wherein said medium further has stored thereon instructions that, when executed, result in the video encoding rate being adjusted by adjusting the quantization step size employed during

video encoding (col.14, ln.9-19; Zhang discloses the coefficient predictor 211 to adjust the quantization step size for properly adjusting the video encoding rate).

Claims 44-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Nickerson (5,926,222).

Regarding claim 44, Nickerson discloses an article (col.2, ln.40-43 and col.4, ln.63-65) comprising:

a storage medium having stored thereon a look up table (col.2, ln.40-52, Nickerson discloses a storage medium that has one or more quantization lookup tables, as illustrated by elements 502, 504, 508, 510, 514 of fig.5, where fig.5 is a detailed illustration of bit-rate estimator element 310 of fig.3), said table comprising a relationship between the number of bits and variation in pixel signal values of a plurality of video images for a variety of quantization step sizes (col.6, ln.49-67, in fig.3, element 312 uses the data from element 310 where lookup tables are used, as shown in fig.5 which shows the details of element 310, and that element 310 has a table 514 where it takes the number of bits and the variation in pixel signal values into account, and that information is sent to element 312 to generate a set of final Q levels or a set of quantization step sizes to properly encode the video images by adjusting the quantization step sizes to properly change the video encoding bit rate);

wherein said storage medium further includes instructions stored thereon to employ the look up table and a bit budget to perform video encoding rate control (col.4, ln.63-65, Nickerson discloses a processor that performs video encoding by executing instructions on how, what and when to encode the video data; and fig.5 is a detailed

illustration of element 310 of fig.3 where bit-rate estimator uses quantization lookup table, quantization coefficient lookup table, and bit contribution (bit budget) lookup tables to perform video encoding rate control).

Regarding claim 45, Nickerson discloses the article of claim 44, wherein the look up table is employed to perform video encoding rate control when the instructions are executed by a processor (col.4, ln.63-65, Nickerson discloses a processor that performs video encoding by executing instructions on how, what and when to encode the video data; in col.7, ln.64 to col.8, ln. 3 and fig.5 is a detailed illustration of bit-rate estimator element 310 of fig.3 where the bit-rate estimator uses quantization lookup table, quantization coefficient lookup table, and bit contribution lookup tables, as well as the zero-run lookup table with a feedback loop to the bit contribution index generator to perform video encoding rate control).

Regarding claim 46, Nickerson discloses the article of claim 45, wherein the variation in pixel signal values comprises the SAD (col.5, ln.61 to col.6, ln.3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (5,812,195) in view of Howe (5,900,865).

Regarding claims 12-14, Zhang discloses the use of a processor for processing compression of video images (col.8, ln.40-42). Zhang does not specifically disclose wherein the video encoder is implemented in silicon on at least one integrated circuit, wherein the silicon implementation of the video encoder comprises microcode and firmware. However, Howe teaches the video encoder is implemented in silicon on at least one integrated circuit (col.6, ln.57-63 and col.17, ln.33-50; video encoding is implemented in silicon on at least one integrated circuit (IC); also, it is well known in the art that integrated circuit chips are implemented in silicon for processing video encoding/decoding tasks), wherein the silicon implementation of the video encoder comprises microcode (col.14, ln.28-43) and firmware (col.17, ln.65-66). Therefore, it would have been obvious to one of ordinary skill in the art to take Howe's teaching of silicon implementation of a video encoder into Zhang's video compression system for permitting video encoding by use of microcode and firmware via silicon integrated circuits (IC) so as to efficiently encoding video image data in a highly efficient manner. Doing so would ensure compatible, cost-effective, efficient, precise, video encoding and decoding of high quality video images for display (col.3, ln.1-13).

Regarding claim 15, Zhang discloses the use of a processor for processing compression of video images (col.8, ln.40-42). Zhang does not specifically disclose wherein said video encoder is implemented in software capable of executing on a processor. However, Howe teaches the video encoder is implemented in software capable of executing on a processor (col.3, ln.1-13; video encoding software can be applied in a processor). Therefore, it would have been obvious to one of ordinary skill

in the art to take Howe's teaching of implementing video encoding software on a processor into Zhang's video compression system for permitting the execution of software so as to efficiently encoding video image data in a highly efficient manner. Doing so would ensure compatible, cost-effective, efficient, precise, video encoding and decoding of high quality video images for display (col.3, ln.1-13).

Regarding claim 16, Zhang discloses the device of claim 15, wherein said processor comprises a microprocessor (col.7, ln.57-61; fig.1, processor 100 has a microprocessor, where the processor 100 encompasses the video encoder of fig.2, as disclosed in col.8, ln.40-42).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen Wong whose telephone number is (703) 306-5978. The examiner can normally be reached on Mondays to Thursdays from 8am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christopher Kelley can be reached on (703) 305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allen Wong
Examiner
Art Unit 2613

AW
1/6/05